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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,145	02/07/2002	Guy E. Averett	ONS00317	1448
7590	06/29/2005		EXAMINER	
ON Semiconductor			MAGEE, THOMAS J	
Patent Administration Dept - MD A700			ART UNIT	PAPER NUMBER
P.O. Box 62890				2811
Phoenix, AZ 85082-2890			DATE MAILED: 06/29/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/072,145	AVERETT ET AL.
	Examiner	Art Unit
	Thomas J. Magee	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 12 April 2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-11 and 26-33 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) 1-9, and 26-32 is/are allowed.
- 6) Claim(s) 10, 11 and 33 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_\_

## DETAILED ACTION

### ***Claim Objections***

1. Claim 26 is objected to on the basis of a minor informality. The phrase, “*a thermal oxide layer grown on the semiconductor layer to form a seal the opening.*” appears to have a typographical error. Examiner assumes that Applicant meant to recite, “*a thermal oxide layer grown on the semiconductor layer to seal the opening.*” Correction is required.

### ***Claim Rejections – 35 U.S.C. 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 10, 11, and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The terms, “amorphous” and “poly[silicon]” are micro-structural descriptions and not not compositional descriptors. Further, although polysilicon and amorphous silicon may be high resistivity materials, neither are classed as dielectrics. Hence, the limitations, “*the third dielectric layer comprises polysilicon,*” and “*the third dielectric layer comprises amorphous silicon,*” are unclear. Correction and/or clarification is required.

4. Claims 7 and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Within both claims there is no limitation describing or

identifying the second dielectric layer and the relationship to a first and third dielectric layer. Correction and/or clarification is required.

### ***Allowable Subject Matter***

4. Claims 1 – 9, and 26 – 32 are allowed. The prior art of record do not reasonably teach or suggest, either singularly or in combination, the limitation in Claim 1 of a semiconductor device comprising "*a semiconductor substrate having a surface formed with a first recessed region; a first dielectric material deposited in the first recessed region and formed with a second recessed region having walls; a semi-conductor layer formed in proximity to the second recessed region; and a thermal oxide layer formed integral with the semiconductor layer, wherein the thermal oxide layer seals the second recessed region while leaving a void in the second recessed region.*"

In like fashion, the prior art of record do not reasonably teach or suggest, either singularly or in combination, the limitation in Claim 26 of a semiconductor device comprising, "*a semiconductor substrate having a surface formed with a first recessed region; a first dielectric material deposited in the first recessed region and formed with a second recessed region having an opening and walls; a semiconductor cap layer formed adjacent the opening; and a thermal oxide layer grown on the semiconductor layer to seal the opening.*"

### ***Conclusions***

5. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272-1658**. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732**. The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306**.

Thomas Magee  
June 2, 2005

Steven Loke  
Primary Examiner

